What is claimed is:

1. A gate stack, comprising:

a tunnel medium;

a high K charge blocking and charge storing medium disposed on the tunnel medium; and

an injector medium operably disposed with respect to the tunnel medium and the high K charge blocking and charge storing medium to provide charge transport by enhanced tunneling.

2. The gate stack of claim 1, wherein the injector medium is disposed on the high K charge blocking and charge storing medium.

3. The gate stack of claim 1, wherein the tunnel medium is disposed on the injector medium.

4. The gate stack of claim 1, wherein the tunnel medium includes tunnel Al_2O_3.

5. The gate stack of claim 1, wherein the tunnel medium includes tunnel SiO_2.

6. The gate stack of claim 1, wherein the high K charge blocking and charge storing medium includes a high K charge blocking medium disposed on a high K charge storing medium with nano crystals.

7. The gate stack of claim 1, wherein the high K charge blocking and charge storing medium includes silicon-rich Al_2O_3.

8. The gate stack of claim 1, wherein the high K charge blocking and charge storing medium includes tantalum.

9. The gate stack of claim 1, wherein the high K charge blocking and charge storing medium includes titanium.

10. The gate stack of claim 1, wherein the high K charge blocking and charge storing medium includes zirconium.

11. The gate stack of claim 1, wherein the high K charge blocking and charge storing medium includes hafnium.

12. The gate stack of claim 1, wherein the high K charge blocking and charge storing medium includes praseodymium.

13. The gate stack of claim 1, wherein the high K charge blocking and charge storing medium includes BST.

14. The gate stack of claim 1, wherein the injector medium includes injector SRN.

15. The gate stack of claim 1, wherein the injector medium includes injector SRO.

16. The gate stack of claim 1, wherein the injector medium includes silicon rich aluminum nitride.

17. The gate stack of claim 1, wherein the tunnel medium, the high K charge blocking and charge storing medium, and the injector medium are scalable with power supply and lithography scaling.

18. A gate stack, comprising:

a tunnel medium;

a high K charge blocking and charge storing medium disposed on the tunnel medium, wherein the high K charge blocking and charge storing medium includes nano crystals for providing charge trapping charge centers; and

an injector medium operably disposed with respect to the tunnel medium and the high K charge blocking and charge storing medium to provide charge transport by enhanced tunneling.

19. The gate stack of claim 18, wherein the nano crystals include silicon nano crystals.

20. The gate stack of claim 18, wherein the nano crystals include gold nano crystals.

21. The gate stack of claim 18, wherein the nano crystals include tungsten nano crystals.

22. The gate stack of claim 18, wherein the nano crystals include silicided nano crystals.

23. A gate stack, comprising:

a first injector medium;

a tunnel medium disposed on the first injector medium;

a high K charge blocking and charge storing medium disposed on the tunnel medium; and

a second injector medium disposed on the high K charge blocking and charge storing medium.

24. The gate stack of claim 23, wherein the first injector medium is disposed on a NO surface treated substrate.

25. The gate stack of claim 23, wherein the first injector medium is disposed on a NH_3 surface treated substrate.

26. The gate stack of claim 23, wherein the tunnel medium is selected from the group consisting of tunnel Al_2O_3 and tunnel SiO_2.

27. The gate stack of claim 23, wherein the injector medium is selected from the group consisting of injector SRN, injector SRO, and silicon rich aluminum nitride.

28. The gate stack of claim 23, wherein the high K charge blocking and charge storing medium includes Al_2O_3.

29. A gate stack, comprising:

a first injector medium;

a tunnel medium disposed on the first injector medium;

a high K charge blocking and charge storing medium disposed on the tunnel medium, wherein the high K charge blocking and charge storing medium includes nano crystals for providing charge trapping charge centers; and

a second injector medium disposed on the high K charge blocking and charge storing medium.

30. The gate stack of claim 29, wherein the nano crystals include silicon nano crystals.

31. The gate stack of claim 29, wherein the nano crystals include gold nano crystals.

32. The gate stack of claim 29, wherein the nano crystals include tungsten nano crystals.

33. The gate stack of claim 29, wherein the nano crystals include silicided nano crystals.

34. A gate stack, comprising:

a tunnel medium;

a high K charge storing medium disposed on the tunnel medium;

a high K charge blocking medium disposed on the high K charge storing medium; and

an injector medium operably disposed with respect to the tunnel medium, the high K charge storing medium and the high K charge blocking medium to provide charge transport by enhanced tunneling.

35. The gate stack of claim 34, wherein the injector medium is disposed on the high K charge blocking medium.

36. The gate stack of claim 34, wherein the tunnel medium is disposed on the injector medium.

37. The gate stack of claim 34, wherein the tunnel medium is selected from the group consisting of tunnel Al_2O_3 and tunnel SiO_2.

38. The gate stack of claim 34, wherein at least one of the high K charge blocking and the high K charge storing medium is selected from the group consisting of Al_2O_3, tantalum, titanium, zirconium, hafnium, praseodymium and BST.

39. The gate stack of claim 34, wherein the injector medium is selected from the group consisting of injector SRN, injector SRO, and silicon rich aluminum nitride.

40. The gate stack of claim 34, wherein the tunnel medium, the high K charge blocking and charge storing medium, and the injector medium are scalable with power supply and lithography scaling.

41. A gate stack, comprising:

a tunnel medium;

a high K charge storing medium disposed on the tunnel medium, wherein the high K charge storing medium includes nano crystals for providing charge trapping charge centers;

a high K charge blocking medium disposed on the high K charge storing medium; and

an injector medium operably disposed with respect to the tunnel medium, the high K charge storing medium and the high K charge blocking medium to provide charge transport by enhanced tunneling.

42. The gate stack of claim 41, wherein the nano crystals include silicon nano crystals.

43. The gate stack of claim 41, wherein the nano crystals include gold nano crystals.

44. The gate stack of claim 41, wherein the nano crystals include tungsten nano crystals.

45. The gate stack of claim 41, wherein the nano crystals include silicided nano crystals.

46. A gate stack, comprising:

a first injector medium disposed on a substrate;

a tunnel medium disposed on the first injector medium;

a high K charge storing medium disposed on the tunnel medium;

a high K charge blocking medium stored on the high K charge storing medium; and

a second injector medium disposed on the high K charge blocking medium.

47. The gate stack of claim 46, wherein the gate stack is disposed on a NO surface treated substrate.

48. The gate stack of claim 46, wherein the gate stack is disposed on a NH_3 surface treated substrate.

49. The gate stack of claim 46, wherein the first and second injector media include injector SRN.

50. The gate stack of claim 46, wherein the first and second injector media include injector SRO.

51. The gate stack of claim 46, wherein the first and second injector media include silicon-rich aluminum nitride.

52. The gate stack of claim 46, wherein the high K charge storing medium includes silicon nano crystals.

53. The gate stack of claim 46, wherein the high K charge storing medium includes gold nano crystals.

54. The gate stack of claim 46, wherein the high K charge storing medium includes tungsten nano crystals.

55. The gate stack of claim 46, wherein the high K charge storing medium includes silicided tungsten nano crystals.

56. A memory cell, comprising:

a substrate including diffused regions that form a source region and a drain region;

a gate stack disposed on the substrate between the source region and the drain region; and

a gate disposed on the gate stack,

wherein the gate stack includes:

a tunnel medium;

a high K charge blocking and charge storing medium disposed on the tunnel medium; and

an injector medium operably disposed with respect to the tunnel medium and the high K charge blocking and charge storing medium to provide charge transport by enhanced tunneling.

57. The memory cell of claim 56, wherein the injector medium is disposed on the high K charge blocking and charge storing medium.

58. The memory cell of claim 56, wherein the tunnel medium is disposed on the injector medium.

59. The memory cell of claim 56, wherein the tunnel medium includes tunnel Al_2O_3.

60. The memory cell of claim 56, wherein the tunnel medium includes tunnel SiO_2.

61. The memory cell of claim 56, wherein the high K charge blocking and charge storing medium includes a high K charge blocking medium disposed on a high K charge storing medium with nano crystals.

62. The memory cell of claim 56, wherein the high K charge blocking and charge storing medium includes silicon-rich Al_2O_3.

63. The memory cell of claim 56, wherein the injector medium includes injector SRN.

64. The memory cell of claim 56, wherein the injector medium includes injector SRO.

65. The memory cell of claim 56, wherein the injector medium includes silicon rich aluminum nitride.

66. The memory cell of claim 56, wherein the tunnel medium, the high K charge blocking and charge storing medium, and the injector medium are scalable with power supply and lithography scaling.

67. A memory cell, comprising:

a substrate including diffused regions that form a source region and a drain region;

a gate stack disposed on the substrate between the source region and the drain region; and

a gate disposed on the gate stack,

wherein the gate stack includes:

a tunnel medium;

a high K charge storing medium disposed on the tunnel medium;

a high K charge blocking medium disposed on the high K charge storing medium; and

an injector medium operably disposed with respect to the tunnel medium, the high K charge storing medium and the high K charge blocking medium to provide charge transport by enhanced tunneling.

68. The memory cell of claim 67, wherein the injector medium is disposed on the high K charge blocking medium.

69. The memory cell of claim 67, wherein the tunnel medium is disposed on the injector medium.

70. The memory cell of claim 67, wherein the tunnel medium includes tunnel Al_2O_3.

71. The memory cell of claim 67, wherein the tunnel medium includes tunnel SiO_2.

72. The memory cell of claim 67, wherein at least one of the high K charge blocking and the high K charge storing medium includes Al_2O_3.

73. A nonvolatile memory device, comprising:

an array of memory cells operably coupled to a grid of row lines and column lines;

row select circuitry for selecting a row of memory cells; and

column select circuitry for selecting a column of memory cells,

wherein the row select circuitry and the column select circuitry cooperate to select a memory cell in the selected row and the selected column for application of a programming voltage; and

wherein each memory cell includes:

a substrate including diffused regions that form a source region and a drain region;

a gate stack disposed on the substrate between the source region and the drain region; and

a gate disposed on the gate stack,

wherein the gate stack includes:

a tunnel medium;

a high K charge blocking and charge storing medium disposed on the tunnel medium; and

an injector medium operably disposed with respect to the tunnel medium and the high K charge blocking and charge storing medium to provide charge transport by enhanced tunneling.

74. The nonvolatile memory device of claim 73, wherein the injector medium is disposed on the high K charge blocking and charge storing medium.

75. The nonvolatile memory device of claim 73, wherein the tunnel medium is disposed on the injector medium.

76. The nonvolatile memory device of claim 73, wherein the tunnel medium includes tunnel Al_2O_3.

77. The nonvolatile memory device of claim 73, wherein the tunnel medium includes tunnel SiO_2.

78. The nonvolatile memory device of claim 73, wherein the high K charge blocking and charge storing medium includes a high K charge blocking medium disposed on a high K charge storing medium with nano crystals.

79. The nonvolatile memory device of claim 73, wherein the high K charge blocking and charge storing medium includes silicon-rich Al_2O_3.

80. The nonvolatile memory device of claim 73, wherein the injector medium includes injector SRN.

81. The nonvolatile memory device of claim 73, wherein the injector medium includes injector SRO.

82. The nonvolatile memory device of claim 73, wherein the injector medium includes silicon rich aluminum nitride.

83. The nonvolatile memory device of claim 73, wherein the tunnel medium, the high K charge blocking and charge storing medium, and the injector medium are scalable with power supply and lithography scaling.

84. An electronic system, comprising:

a processor; and

a nonvolatile memory device coupled to the processor, the nonvolatile memory device including:

an array of memory cells operably coupled to a grid of row lines and column lines;

row select circuitry for selecting a row of memory cells; and

column select circuitry for selecting a column of memory cells,

wherein the row select circuitry and the column select circuitry cooperate to select a memory cell in the selected row and the selected column for application of a programming voltage; and

wherein each memory cell includes:

a substrate including diffused regions that form a source region and a drain region;

a gate stack disposed on the substrate between the source region and the drain region; and

a gate disposed on the gate stack,

wherein the gate stack includes:

a tunnel medium;

a high K charge blocking and charge storing medium disposed on the tunnel medium; and

an injector medium operably disposed with respect to the tunnel medium and the high K charge blocking and charge storing medium to provide charge transport by enhanced tunneling.

A 85. A method of forming a nonvolatile memory cell, comprising:

providing a tunnel medium;

disposing a high K charge blocking and charge store medium on the tunnel medium; and

operably disposing an injector medium with respect to the tunnel medium and the high K charge blocking and charge storing medium to provide charge transport by enhanced tunneling.

86. The method of claim 85, wherein operably disposing an injector medium includes disposing the injector medium on the high K charge blocking and charge store medium.

87. The method of claim 85, wherein operably disposing an injector medium includes disposing the tunnel medium on the injector medium.

88. The method of claim 85, wherein operably disposing an injector medium includes providing a first injector medium and a second injector medium, wherein providing a second injector medium includes disposing the second injector medium on the high K charge blocking and charge store medium, and wherein providing a tunnel medium includes disposing the tunnel medium on the first injector medium.

89. The method of claim 85, wherein disposing a high K charge blocking and charge storing medium on the tunnel medium includes disposing a high K charge storing medium on the tunnel medium and disposing a high K charge blocking medium on the high K charge storing medium.

90. The method of claim 85, wherein disposing a high K charge blocking and charge storing medium on the tunnel medium includes disposing silicon-rich Al_2O_3 on the tunnel medium.

91. The method of claim 85, wherein operably disposing an injector medium includes disposing injector SRN.

92. The method of claim 85, wherein operably disposing an injector medium includes disposing injector SRO.

93. The method of claim 85, wherein operably disposing an injector medium includes disposing silicon-rich aluminum nitride.

94. The method of claim 85, wherein providing a tunnel medium includes providing tunnel Al_2O_3.

95. The method of claim 85, wherein providing a tunnel medium includes providing tunnel SiO_2.

96. A method of forming a nonvolatile memory cell, comprising:

providing a tunnel medium;

disposing a high K charge blocking and charge store medium on the tunnel medium, including dispersing nano crystals in a high K dielectric; and

operably disposing an injector medium with respect to the tunnel medium and the high K charge blocking and charge storing medium to provide charge transport by enhanced tunneling.

97. The method of claim 96, wherein dispersing nano crystals includes implanting nano crystals.

98. The method of claim 96, wherein dispersing nano crystals includes doping nano crystals.

99. The method of claim 96, wherein dispersing nano crystals includes dispersing silicon nano crystals.

100. The method of claim 96, wherein dispersing nano crystals includes dispersing gold nano crystals.

101. The method of claim 96, wherein dispersing nano crystals includes dispersing tungsten nano crystals.

102. The method of claim 96, wherein dispersing nano crystals includes dispersing silicided tungsten nano crystals.

103. A method of enhancing an electric field across a gate stack in a NV memory cell, comprising:

dispersing nano crystals in a high K dielectric to provide charge trapping charge centers in the high K dielectric; and

providing an injector medium with nano crystals to provide charge transport by enhanced tunneling.

104. The method of claim 103, further comprising providing a contact between a programming electrode and the high K dielectric.

105. The method of claim 103, wherein providing an injector medium includes providing the injector medium between a programming electrode and the high K dielectric.

106. The method of claim 103, wherein providing an injector medium includes providing the injector medium between a tunnel medium and a source electrode.

107. The method of claim 103, wherein providing an injector medium with nano crystals includes providing an injector medium with silicon nano crystals.

108. The method of claim 103, wherein providing an injector medium with nano crystals includes providing an injector medium with gold nano crystals.

109. The method of claim 103, wherein providing an injector medium with nano crystals includes providing an injector medium with tungsten nano crystals.

110. The method of claim 103, wherein providing an injector medium with nano crystals includes providing an injector medium with silicided tungsten nano crystals.

111. The method of claim 103, wherein dispersing nano crystals in a high K dielectric to provide charge trapping charge centers in the high K dielectric includes dispersing silicon nano crystals in Al_2O_3 to form silicon-rich Al_2O_3.

112. The method of claim 103, further comprising providing a high K charge blocking medium and providing a high K charge storing medium, wherein dispersing nano crystals in a high K dielectric forms the high K charge storing medium, and wherein providing a high K charge blocking medium includes disposing the high K charge blocking medium on the high K charge storing medium.

113. The method of claim 112, wherein providing a high K charge blocking medium includes providing blocking Al_2O_3, and wherein providing a high K charge storing medium includes providing silicon-rich Al_2O_3.

114. A method of operating a nonvolatile memory device, comprising:

writing to one or more non-volatile memory cells in one or more arrays by applying a voltage across a high K dielectric to store charge on charge centers in the high K dielectric; and

erasing one or more non-volatile memory cells by applying a voltage across the high K dielectric to tunnel electrons off of the charge centers.

115. The method of claim 114, wherein applying a voltage across a high K dielectric includes enhancing a resulting electric field using at least one injector medium.

116. The method of claim 114, wherein writing to one or more non-volatile memory cells in one or more arrays includes applying a voltage across alumina (Al_2O_3) to store charge on charge centers formed by nano crystals dispersed in the Al_2O_3.

117. An electronic system, comprising:

a plurality of fixed threshold devices for performing random logic functions; and

a plurality of nonvolatile devices operably coupled to the plurality of fixed threshold devices to provide desired logic functions, wherein each of the plurality of nonvolatile devices includes:

a substrate including diffused regions that form a source region and a drain region;

a gate stack disposed on the substrate between the source region and the drain region; and

a gate disposed on the gate stack,

wherein the gate stack includes:

a tunnel medium;

a high K charge storing medium disposed on the tunnel medium;

a high K charge blocking medium disposed on the high K charge storing medium; and

an injector medium operably disposed with respect to the tunnel medium, the high K charge storing medium and the high K charge blocking medium to provide charge transport by enhanced tunneling.

118. The electronic system of claim 117, wherein the plurality of fixed threshold devices include an input node, and the plurality of nonvolatile devices are operably coupled to the input node to provide the desired logic functions.

119. The electronic system of claim 118, wherein the plurality of fixed threshold devices and the plurality of nonvolatile devices are deployed as an alterable logic device (ALD).

120. The electronic system of claim 118, wherein the plurality of fixed threshold devices and the plurality of nonvolatile devices are deployed as a programmable logic device (PLD).

121. The electronic system of claim 117, wherein the plurality of fixed threshold devices include an output node, and the plurality of nonvolatile devices are operably coupled to the output node to provide the desired logic functions.

122. The electronic system of claim 121, wherein the plurality of fixed threshold devices and the plurality of nonvolatile devices are deployed as an alterable logic device (ALD).

123. The electronic system of claim 121, wherein the plurality of fixed threshold devices and the plurality of nonvolatile devices are deployed as a programmable logic device (PLD).

124. An electronic system, comprising:

a programmable logic array; and

a nonvolatile programmable memory array (NVPMA) coupled to the programmable logic array, wherein the NVPMA includes a plurality of logic devices, each of the plurality of logic devices including:

a substrate including diffused regions that form a source region and a drain region;

a gate stack disposed on the substrate between the source region and the drain region; and

a gate disposed on the gate stack,

wherein the gate stack includes:

a tunnel medium;

a high K charge storing medium disposed on the tunnel medium;

a high K charge blocking medium disposed on the high K charge storing medium; and

an injector medium operably disposed with respect to the tunnel medium, the high K charge storing medium and the high K charge blocking medium to provide charge transport by enhanced tunneling.